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PRE-APPEAL BRIEF REQUEST FOR REVIEW		Docket Number (Optional)
		SCS-550-530
	Application Number	Filed
	10/798,890	March 12, 2004
	First Named Inventor	
	BURDASS	
	Art Unit	Examiner
	2183	B. Johnson
<p>Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.</p> <p>This request is being filed with a notice of appeal.</p> <p>The review is requested for the reason(s) stated on the attached sheet(s). Note: No more than five (5) pages may be provided.</p> <p>I am the</p> <p><input type="checkbox"/> Applicant/Inventor</p> <p><input type="checkbox"/> Assignee of record of the entire interest. See 37 C.F.R. § 3.71. Statement under 37 C.F.R. § 3.73(b) is enclosed. (Form PTO/SB/96)</p> <p><input checked="" type="checkbox"/> Attorney or agent of record <u>27,393</u> (Reg. No.)</p> <p><input type="checkbox"/> Attorney or agent acting under 37CFR 1.34. Registration number if acting under 37 C.F.R. § 1.34 _____</p> <p>NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.*</p> <p><input checked="" type="checkbox"/> *Total of 1 form/s are submitted.</p>		
		 Signature Stanley C. Spooner _____ Typed or printed name 703-816-4028 _____ Requester's telephone number February 27, 2007 _____ Date

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STATEMENT OF ARGUMENTS IN SUPPORT OF
PRE-APPEAL BRIEF REQUEST FOR REVIEW

The following listing of clear errors in the Examiner's rejection and his failure to identify essential elements necessary for a *prima facie* basis of rejection is responsive to the Final Rejection mailed November 27, 2006 (Paper No. 20061120).

Error #1. The Examiner fails to identify where the Birk reference teaches "upon completion of execution of said current program instruction . . ." said instruction prefetch unit fetches said exception handling program instructions

Applicant's independent claims 9 and 24 both specify the conditional phrase that upon "completion of execution of said current program instruction" other actions take place. This is not correct in the Birk reference. The Examiner not only fails to disclose where this claimed conditional element is taught in Birk, he apparently fails to appreciate the Birk actually teaches the direct opposite of this claim requirement.

Birk at column 3, lines 59-63, states that "since the DSP 10 aborts the instructions in the pipeline upon detection of an interrupt, it aborts the instruction which generated the cache line miss and begins execution of the interrupt service routine." (emphasis added). Accordingly, the instruction is not completed, and this failure to complete is necessary for the proper operation of the Birk reference. Birk does not explain how it is able to tolerate aborting such a partially completed instruction.

As explained in detail on page 4, lines 1-12 of the present specification, the claimed invention initiates the cache line fill operation to read the exception handling program instruction from main memory partway through execution of the current program instruction, but does not fetch that instruction from the cache memory until completion of the current program instruction. Thus,

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Birk, which teaches instruction abortion, clearly does not have Applicant's claimed exception controller which is dependent upon "completion of execution of said current program instruction." (emphasis added).

Thus, the Examiner has not indicated how or where the Birk reference teaches Applicant's conditional controller, i.e., "upon completion of execution of said current program instruction." Clearly, the Birk reference requires the direct opposite of Applicant's claimed exception controller which requires abortion of "the instructions in the pipeline upon detection of an interrupt." (Column 3, lines 60-61).

Since the Examiner has failed to demonstrate where this aspect of claims 9 and 24 exists in the Birk reference, the rejection of independent claims 9 and 24 and claims 10-12 and 25-27 dependent thereon as being anticipated by Birk is clearly not supported.

Error #2. The Examiner's assertion on page 3, first full paragraph is completely unsupported by the Birk reference

The Examiner states on page 3 that "Note that the instruction service routine comprises a plurality of instructions. So, it follows the memory hierarchy outlined in col 2 lines 36-49." This contention by the Examiner is traversed and, in fact, is contrary to what one of ordinary skill in the art would understand when reading the Birk reference.

The whole point of the Birk disclosure is to avoid the stall cycles associated with a miss in the cache memory. Instead, Birk suggests that when executing a normal program instruction from a given program thread, if a miss occurs, then this should trigger processing to be started from another program thread so that the stall associated with the cache miss can be avoided. In order to achieve this desired behavior, which is the whole reason for the arrangement of Birk, it is necessary that the instruction of the ISR or the different thread should be present within the

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cache memory and not itself result in a second cache miss. There is no point in the system of Birk if one cache miss is avoided merely to result in another cache miss. It will be appreciated by those in the field that Birk could readily arrange for the ISR or other thread code to be guaranteed present within the memory by, for example, using a cache lockdown technique for such code. The assertion by the Examiner that the interrupt service routine will follow the normal memory hierarchy within Birk and accordingly will require fetching to the cache memory is unsupported and in fact contrary to the purpose of Birk.

Thus, the Examiner's conclusion that Birk teaches a plurality of instructions which will follow the memory hierarchy outlined in column 2, lines 36-49 is simply wrong and actually contrary to the disclosure contained in Birk. Again, if Birk contained any such disclosure, the Examiner would be able to point to that disclosure as an example. The Examiner has failed to so indicate and therefore fails to meet his burden of proving a *prima facie* case of anticipation and/or obviousness with respect to the independent claims.

Error #3. The Examiner appears to ignore the "if . . . , then . . ." conditionality which is expressed in claims 9 and 24

The Examiner construes this claim language to be met if, as he argues the Birk teaching discloses, the behavior takes place both if the exception is still current and if the exception is not still current. This is believed to be an improper interpretation of this portion of Applicant's claim.

The claim language positively recites "upon completion of execution of said current program instruction, **if said exception is still current, then said instruction prefetch unit fetches . . .**" The Examiner has provided no support for his misinterpretation of the claim language which clearly states that "if said exception is still current, then said instruction prefetch

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unit fetches." There is certainly no identification that an exception controller having this aspect is disclosed in the Birk reference and therefore Birk fails to anticipate the independent claims 1 & 24 as well as those dependent thereon.

Error #4. The Examiner provides no "reason" or "motivation" for combining the Birk and secondary references

The rejection of claims 13 and 28 requires a combination of Birk and Nguyen and the rejection of claims 14, 15, 29 and 30 requires the combination of Birk and Glass. As is well known, examiners are not free to merely pick and choose elements from different references and combine them in the manner taught only by applicant's claims. Rather, the Court of Appeals for the Federal Circuit has consistently held that the burden is on the examiner to establish some "reason" or "motivation" for combining elements of two prior art references.

While the requirement for some "reason" or "motivation" for combining elements was pointed out to the Examiner (previous amendment page 10), the Examiner's statement that one skilled in the art would have been motivated to make the combination based on the reasoning disclosed in Glass (i.e., that an integrated circuit is "highly advantageous for space, speed, power consumption and cost reasons" (Glass, column 4, lines 23-25)) does not provide any reason or motivation. Using an integrated circuit does provide some of the stated advantages, but the Examiner has not indicated how or where there is any reason or motivation to pick and chose the elements from the Birk/Glass or Birk/Nguyen combinations of references and combine them in the manner of Applicant's claims. While some advantages of integrated circuits are identified, the required reason and motivation for combining elements is still missing.

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Error #5. The Examiner ignores the fact that Birk teaches away from Applicant's claimed combination

As noted above, Birk teaches the abortion of the instruction which generated the cache line miss and thus the instruction is not completed. As noted, this is the direct opposite of Applicant's claimed requirement "upon completion of execution of said current program instruction." (emphasis added). Thus, Birk, in teaching the direct opposite of Applicant's claimed exception controller, would tend to lead one of ordinary skill in the art away from Applicant's invention.

The Examiner has failed to explain how or why one of ordinary skill in the art would ignore this contrary teaching of Birk when attempting to make the combination of Birk with either Nguyen or Glass in the rejections of claims 13-15 and 28-30. As a consequence, neither of these combinations would be obvious in view of the Birk reference.

SUMMARY

Claimed structure and method steps are not identified as being disclosed or present in the Birk reference. The Examiner fails to identify where the Birk reference teaches "upon completion of execution of said current program instruction . . ." (claim 1, line 12 and claim 24, line 14), or the conditional phrase "if said exception is still current, then . . ." (claim 1, line 13 and claim 24, lines 14-15). The Examiner has ignored the requirements to show both a reason for combining prior art as well as some rationale for ignoring contrary teachings.

As a result of the above, there is simply no support for the rejection of Applicant's independent claims 1 and 24 or claims dependent thereon under 35 USC §102 and/or §103. Applicant respectfully requests that the Pre-Appeal Panel find that the application is allowed on the existing claims and prosecution on the merits should be closed.